MEMRISTIVE DEVICE OPTIMIZATION TOWARDS SPIKING NEUROMORPHIC SYSTEMS

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Hardware spiking neural networks (SNNs) hold the great promise of a brain-inspired and efficient online processing of real-world signals impacting fields like edge-computing, robotics and prosthetics.
Resistive memory devices and memristive devices, i.e. metal/insulator/metal devices that undergo resistance change upon voltage application, have been acknowledged as key-enabling technology for hardware neural networks. In fact, they have to potential to work as synapses enabling high interconnectivity among neurons, plasticity and adaptation. However, the long-standing research on these devices have evidenced their strengths and limitations and various existing performances trade-offs. Furthermore, memristors in SNNs are used in a somewhat unconventional manner, because of system-level or algorithmic constraints.
For these reasons, it is becoming more and more evident that a co-engineering of devices and networks is needed for a breakthrough in the neuromorphic field to be fulfilled.
In this perspective, we developed non-volatile memristive devices based on HfO_2 layers able to show analogue plasticity evidencing strengths and limitations in their dynamics, variability and noise which are intrinsic to the physics of the operation. We further analyse these aspects in system-level by simulations of neural networks based on equation derived from CMOS circuits and real devices, thus moving some first steps towards a co-engineering of devices and systems.

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