# A MULTISCALE APPROACH TO IDENTIFY TRAPS RESPONSIBLE FOR SUBTHRESHOLD CONDUCTION AND THRESHOLD SWITCHING IN OTS MATERIALS

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We propose a multiscale approach that combines experiments and device simulations to identify the active traps in chalcogenide materials for OTS application and connects them to the observed subthreshold conduction and threshold switching. The methodology relies on the accurate analysis and simulation (performed with the Ginestra® platform [1]) of carriers trapping and transport (defect-assisted, tunnelling, drift, hydrodynamic) to reproduce voltage, frequency and temperature dependence of multiple electrical characteristics, and is schematically represented in Figure 1. Figure 2 shows the excellent agreement between experiments and simulations obtained for current (I-V) and conductance (G-V) data measured on samples with 20nm-thick $Ge_{60}Se_{40}$ and $Ge_{50}Se_{50}$ films. Both devices exhibit a p-type conduction through a defect band located in the lower portion of the band-gap (compatible with Selenium vacancy traps), as seen from the extracted defect maps in Figure 2(c),(f). Moreover, the bandgap is found to reduce with the Ge content (1.45eV for $Ge_{50}Se_{50}$ and 1.1eV for $Ge_{60}Se_{40}$), in agreement with DFT results [2]. A correct characterization of GeSe traps is critical to properly model not only sub-threshold conduction, but also threshold switching. Figure 3 shows an example of current- and voltage-driven OTS characteristics simulated for a 20nm-thick $Ge_{50}Se_{50}$ device. The current-driven response (red line) highlights three different conductive regions that are self-consistently simulated considering the extracted trap properties and the developed physical model for OTS conduction (coupling trap-assisted transport, TAT, and hydrodynamic theory): 1) an OFF state at low fields due to TAT with no carrier heating; 2) a switching regime characterized by electric-field induced carrier heating (carriers fail to entirely relax their excess energy to the lattice) that allows them to sustain higher currents with lower fields, thus leading to the observed voltage-snapback; 3) a high current ON state where a hot percolation path is formed that sustains the entire current. The OTS switching modelling based on traps extracted adopting the proposed methodology well reproduces both OFF and ON states and switching voltage for GeSe films with varying composition (not shown).

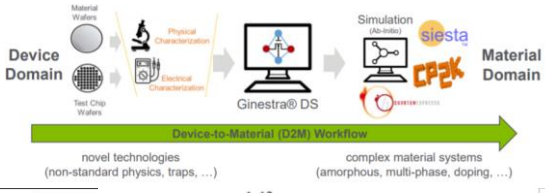


**Figure 1**. Schematic representation of the proposed methodology. (left to right) Electrical data measured on material blankets/test chips are given as input to the Ginestra® simulation platform. Experimental data are reproduced to extract relevant material parameters and trap energy/space distribution. DFT tools and material properties databases can then be used to identify the atomic structure and nature of the extracted traps.

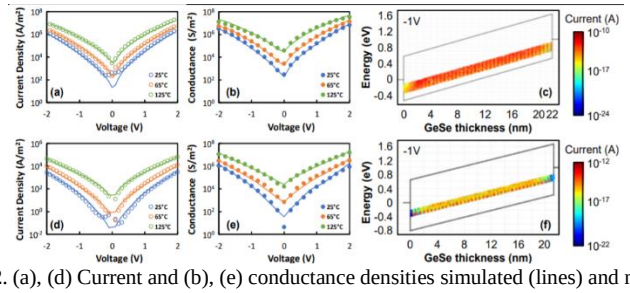


**Figure 2**. (a), (d) Current and (b), (e) conductance densities simulated (lines) and measured (symbols) at different temperatures on 20nm-thick (top row) TiN/Ge60Se40/TiN and (bottom row) TiN/Ge50Se50/TiN capacitors. (c), (f) Corresponding trap distributions as extracted by applying the proposed methodology.

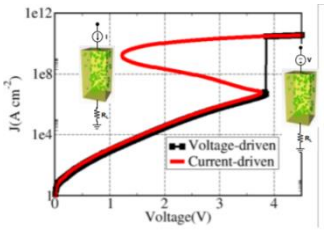


**Figure 3.** Example of J-V curves simulated for a 20nm-thick GeSe OTS under (black line) voltage-driven and (red line) current-driven modes.

**Keywords** Ginestra®, OTS switching, GeSe, trap characterization.
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**References**

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